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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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LSI CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
CHOU, ALBERT T	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/624,264	ORBERK ET AL.	
	Examiner	Art Unit	
	Albert T. Chou	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2007 for the amendment*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The following is a response to the amendment filed on June 25, 2007.

- Claims 1-16 are pending in the application.
- Claims 1, 2, 9 and 10 remain rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 7,043,651 by Aweya et al. (hereinafter "Aweya").
- Claims 3-6 and 13-16 remain rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,043,651 by Aweya in view of US Patent Application Pub. No. 2006/0062195 A1 by Gervais et al. (hereinafter "Gervais").
- Claims 7 and 8 remain rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,043,651 by Aweya in view of US Patent Application Pub. No. 2006/0062195 A1 by Gervais and further in view of US Patent Application Pub. No. 2006/0109059 A1 by Skerritt et al. (hereinafter "Skerritt").
- Claims 11 and 12 remain rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,043,651 by Aweya in view of US Patent Application Pub. No. 2006/0109059 A1 by Skerritt.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 7,043,651 by Aweya et al. (hereinafter "Aweya").

Regarding claims 1 and 9, Aweya teaches a method and an apparatus for controlling the frequency of oscillation of a local clock signal comprising the steps of and means for:

(A) generating said local clock signal **[Fig. 4; Local Clock Signal/Receiver Frequency fs(n)]** in response to a first control signal **[Fig. 4; A u(n) control signal]**;

(B) generating said first control signal **[Fig. 4; A u(n) control signal]** in response to one of a plurality of adjustment signals selected in response to a second control signal **[Fig. 4; An e(n) control signal]**; and

(C) generating said second control signal **[Fig. 4; An e(n) control signal]** in response to a comparison between a local timestamp **[Fig. 4; delta R(n) or R(n)]** and an external timestamp **[Fig. 4; delta T(n) or T(n)]**, wherein said second control signal

selects said one of the plurality adjustment signals **[Fig. 4; one of e(n) error/control signal values]** when a difference between said local time stamp and said external timestamp is outside a predefined margin **[Fig. 4; it is inherent in PLL 50 to generate and select an error signal e(n) value, i.e. the second control signal, which is a variable and the value is determined by the difference between the transmitter timestamp difference delta T(n) and the receiver timestamp difference delta R(n), so long as the error signal e(n) has, for example, a non-zero value, i.e. outside the predetermined zero error margin; col. 8, lines 39-53]**.

Regarding claim 2, Aweya teaches said second control signal is generated in further response to said local clock signal **[Fig. 4; An e(n) control signal is in response to the Local Clock Signal fs(n)]**.

Regarding claim 10, Aweya teaches an apparatus **[Fig. 4]** comprising:

an oscillator configured to generate a clock signal **[Fig. 4; A DCO 60 generates a Local Clock Signal fs(n)]** in response to a first control signal **[Fig. 4; A u(n) control signal]**;

an adjustment circuit configured to generate said first control signal **[Fig. 4; e.g. Circuits associated with differencing elements 42, 54, 56, 66, Loop Filter 58, DCO 60, etc. to generate a u(n) control signal]** in response to one of a plurality of adjustment signals selected in response to a second control signal **[Fig. 4; An e(n) control signal]**; and

a tuning circuit configured to generate said second control signal **[Fig. 4; e.g. Circuits associated with differencing elements 42, 54, 56, 66 etc. to generate an e(n) control signal]** in response to a comparison between a local timestamp **[Fig. 4; delta R(n) or R(n)]** and an external timestamp **[Fig. 2; delta T(n) or T(n)]**, wherein said second control signal selects said one of the plurality adjustment signals **[Fig. 4; one of e(n) error/control signal values]** when a difference between said local time stamp and said external timestamp is outside a predefined margin **[Fig. 4; it is inherent in PLL 50 to generate and select an error signal e(n) value, i.e. the second control signal, which is a variable and the value is determined by the difference between the transmitter timestamp difference delta T(n) and the receiver timestamp difference delta R(n), so long as the error signal e(n) has, for example, a non-zero value, i.e. outside the predetermined zero error margin; col. 8, lines 39-53]**.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,043,651 by Aweya et al. (hereinafter "Aweya") in view of US Patent Application Pub. No. 2006/0062195 A1 by Gervais et al. (hereinafter "Gervais").

Regarding claims 3-6 and 13-16, Aweya teaches each limitation set for in its parent claim.

Aweya does not expressly teach said external timestamp comprises an extracted headend timestamp, wherein said extracted headend timestamp is embedded in a digital bitstream received from a satellite, wherein said local timestamp comprises timing information in a satellite set-top box, a computer readable medium configured to store instructions to execute steps for controlling a satellite set top box.

Gervais teaches said external timestamp comprises an extracted headend timestamp, wherein said extracted headend timestamp is embedded in a digital bitstream received from a satellite **[Fig. 1; Satellite 104, Headend 116, digital packets 116 containing headend timestamp 118; CPU/Demux extracts the timestamps; pars, 0020, 0021 &0029]**, wherein said local timestamp comprises timing information in a satellite set-top box **[Fig. 1; a satellite Set Top Box 120 & a local Clock/VCXO 124]**.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement a clock synchronization mechanism used in a wired network system as disclosed by Aweya to a wireless system such as a satellite headend/set box system as disclosed by Gervais since both wired and wireless systems require an accurate frequency on a voltage or digital controlled oscillator.

The motivation for combining the reference teachings would be to easily apply the widely used and reliable clock synchronization mechanism in the packet networks to the increasing demand of high quality real-time multimedia applications requiring strict clock synchronization properties, such as digital television programs transmitted by the satellite, since a good clock synchronization scheme is essential for the successful deployment of digital wireless communications.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,043,651 by Aweya et al. (hereinafter "Aweya") in view of US Patent Application Pub. No. 2006/0062195 A1 by Gervais et al. (hereinafter "Gervais") and further in view of US Patent Application Pub. No. 2006/0109059 A1 by Skerritt et al. (hereinafter "Skerritt").

Regarding claims 7 and 8, Aweya teaches each limitation set for in its parent claim.

Aweya does not expressly teach a computer readable medium configured to store instructions to execute steps for controlling the frequency of oscillation of a local clock signal and the instructions are further configured to execute steps for controlling a satellite set top box.

Gervais teaches the steps for controlling the frequency of oscillation of a local clock signal for controlling a satellite set top box **[Fig. 1; a satellite Set Top Box 120 & a local Clock/VCXO 124]**. Skerritt also teaches a method and a system for maintaining an accurate frequency of oscillation of a local clock signal **[Fig. 2; pars. 0021-0027]**. Skerritt further teaches a computer readable medium configured to store instructions to execute steps for controlling the frequency of oscillation of a local clock signal **[Fig. 10; pars. 0046-0053]**.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement a clock synchronization mechanism used in a wired network system as disclosed by Aweya to a wireless system such as a satellite headend and a set top box system as disclosed by Gervais, and, to further implement the steps of the clock synchronization mechanism, using the combination of hardware and software, which may be stored in a computer-readable medium program and loaded into a computer system for execution as disclosed by Skerritt,

The motivation for combining the reference teachings would be to easily apply the widely used and reliable clock synchronization mechanism in the packet networks to the increasing demand of high quality real-time multimedia applications requiring strict clock synchronization properties, such as digital television programs transmitted by a

satellite, since a good clock synchronization scheme is essential for the successful deployment of digital wireless communications.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,043,651 by Aweya et al. (hereinafter "Aweya") in view of US Patent Application Pub. No. 2006/0109059 A1 by Skerritt et al. (hereinafter "Skerritt").

Regarding claims 11 and 12, Aweya teaches each limitation set for in its parent claim.

Aweya does not expressly teach said plurality of adjustment signals comprise multiplexer configuration signals, and said adjustment circuit comprises (i) a processor configured to generate said first control signal and (ii) memory configured to store instructions for generating said first control signal.

Skerritt teaches said plurality of adjustment signals comprise multiplexer configuration signals **[Fig. 2; MUX 206; pars. 0021, 0024 & 0025]**, and said adjustment

circuit comprises (i) a processor configured to generate said first control signal **[Fig. 2; Generation Circuit 214; pars. 0021-0027]** and (ii) memory configured to store instructions for generating said first control signal **[Fig. 10; pars. 0046-0053]**.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to implement a clock synchronization mechanism as disclosed by Aweya by using the combination of hardware and software, which may be stored in a computer-readable medium program and loaded into a computer system for execution, as disclosed by Skerritt.

The motivation for combining the reference teachings would be to easily apply the clock synchronization mechanism in the packet networks to the increasing demand of high quality real-time multimedia applications requiring strict clock synchronization properties, such as digital television programs transmitted by a satellite headend and set top boxes installed in most of homes, since a good clock synchronization scheme is essential for the successful deployment of a satellite headend and set top box system.

Response to Remarks

6. Applicant's remarks and amendments filed June 25, 2007 to overcome the rejection of claims 1, 9, 10 and their respective dependent claims in the application have been fully considered but they are not persuasive.

Regarding claims 1, 9 and 10, Applicants argue that Aweya does not disclose or suggest "*The second control signal selects said one of a plurality of adjustment signals*

when a difference between the local time stamp and the external timestamp is outside a predefined margin". Examiner respectfully disagrees.

Aweya teaches the function of the improved PLL 50 is to control the local clock frequency of the receiver such that the error signal e(n), i.e. the second control signal, equals zero, at which point the local clock frequency of the receiver equals to the local clock frequency of the transmitter. This is accomplished by making the difference between the transmitter timestamp difference delta T(n) and the receiver timestamp difference delta R(n) to equal zero **[Fig. 4, col. 8, lines 39-53. i.e. a predetermined margin]**. This means that PLL 50 inherently generates and selects an error signal e(n) value, i.e. the second control signal as recited in claims 1, 9 and 10, which is a variable and the value is determined by the difference between the transmitter timestamp difference delta T(n) and the receiver timestamp difference delta R(n), so long as the error signal e(n) has, for example, a non-zero value, i.e. outside the predetermined zero error margin. Thus Aweya's teachings meet each limitation set forth in claims 1, 9 and 10.

Claims 2-8 and 11-16 depend from claims 1 and 10, respectively. In addition to the basis of rejection to claims 1 and 10, they remain rejected under 35 U.S.C. 102(e) or 35 U.S.C. 103(a) as recited in Sections 1-5 of this office action.

It is concluded that Aweya's reference in its entirety does anticipate claims 1, 2, 9 and 10. Aweya's reference, in combination with Gervais' reference, obviates claims 3-6

and 13-16, Aweya's reference, in combination with Gervais' and Skerritt's references, obviates claims 7 and 8, and Aweya's reference, in combination with Skerritt's reference, obviates claims 11 and 12. Therefore, claims 1-16 are not allowable over these references.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert T. Chou whose telephone number is 571-272-6045. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Albert T. Chou
July 15, 2007 AC

CHI PHAM
SUPERVISORY PATENT EXAMINER
7/16/07